

REMARKS

At the time of the Office Action dated May 18, 2004, claims 1-10 were pending. Applicants acknowledge, with appreciation, the Examiner's indication that claims 3 and 6-10 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 1, 2, 4 and 5 stand rejected.

In this Amendment, claims 1 and 5 have been amended and new claim 11 added. Care has been exercised to avoid the introduction of new matter. Adequate descriptive support for the amendment of claim 1 can be found on, for example, page 45, lines 10-20 and page 50, lines 17-28 of the specification. Adequate descriptive support for new claim 11 can be found on, for example, page 8, lines 8-18 of the specification. The amendment of claim 5 has been made to improve wording.

Specification.

The Examiner advised amending the specification because of informalities. In response, Applicants have amended the specification, as attached, in a manner suggested by the Examiner, except the reference "SRFEXT" on page 29, line 17 of the specification. In this Amendment, Fig. 10 has been amended to replace "SRFEXI" with --SRFEXT--, instead of replacing the reference "SRFEXT" on page 29, line 17 of the specification with --SRFEXI--. Accordingly, withdrawal of the objections to the specification is respectfully solicited.

Claims 5 has been rejected under 35 U.S.C. §112, second paragraph, as being indefinite.

The Examiner pointed out that there is insufficient basis for the limitation “said data holding mode instruction signal” in claim 5. In response, claim 5 has been amended to obviate that issue. Therefore, Applicants respectfully solicit withdrawal of the rejection of claim 5.

Claims 1, 2, 4 and 5 have been rejected under 35 U.S.C. §102(b) as being anticipated by Ooishi.

In the statement of the rejection, the Examiner asserted that Ooishi discloses a semiconductor circuit device with reduced power consumption in slow operation mode identically corresponding to what is claimed.

It is established that the factual determination of lack of novelty under 35 U.S.C. §102 requires the identical disclosure in a single reference of each element of the claimed invention, such that the identically claimed invention is placed into the possession of one having ordinary skill in the art. *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F. 3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994).

Based on the above legal tenet, Applicants submit that Ooishi does not disclose a semiconductor memory device including all the limitations recited in claim 1, as amended. Specifically, the reference does not disclose a semiconductor memory device including “a bit line isolation control circuit for setting at least the bit line isolation circuit provided for a specific memory block to be nonconductive in a standby mode of operation, said specific memory block invariably being designated,” (emphasis added).

Before discussing differences between the claimed invention and the prior art, Applicants briefly explain a standby mode of operation. The standby mode of operation covers the state in which a memory cell is in a non-selected state, or a signal RAS (row address strobe signal) is in an inactive state in a normal mode and in a self refresh mode. In the self refresh mode, a memory cell is selected to have storage data refreshed at predetermined intervals, and a memory cell is in a non-selected state or in a standby state between refresh periods. That is, the operation cycle in the self refresh mode includes an active cycle and a standby cycle.

In the claimed invention, a memory block to be isolated from a corresponding sense amplifier band in the standby cycle is fixedly determined and not changed in progress of the operation (“said specific memory block invariantly being designated” recited in claim 1, as amended). In more detail, a memory block having a bit line short circuit failure is disconnected from a corresponding sense amplifier in the standby cycle both in the normal mode of operation and the self refresh mode. Thus, current consumption is reduced in the standby state.

Ooishi discloses its operation in the standby state with reference to Fig. 34 as follows:

In standby state, the potentials of bit line select signals BLI1 and BLI2 both attain the level of boosted power supply potential. Therefore, bit line pairs BL and /BL at both sides are connected to one sense amplifier 338. If memory block B1, for example, is selected, the potential of bit line select signal BLI2 is lowered. As a result, bit line pair BL and /BL in memory block B2 is disconnected from sense amplifier 338. Column 27, lines 43-50.

In the above paragraph, Ooishi discloses a shared sense amplifier arrangement, in which a memory block is connected to a corresponding sense amplifier band in the standby cycle, and a memory block (non-selected memory block) paired with a selected memory block is isolated from a corresponding sense amplifier band in the active cycle in the normal mode of operation. It is noted that the normal mode of operation indicates an operation mode in which external data access is made to the memory device.

The operation cycle in the self refresh mode includes an active cycle (selected for refreshing storage data) and a standby cycle (not selected for refreshing storage data). For example, in the self refresh mode in which data retention is performed and no external data access is made (the active cycle in the self refresh mode), a selected memory block in Ooishi is normally connected to a corresponding sense amplifier band, and a paired non-selected memory block is isolated from the corresponding sense amplifier band. Thus, Ooishi discloses that a particular memory block is isolated from the corresponding sense amplifier band in the standby cycle.

However, again, Ooishi does not disclose that a memory block to be isolated from a corresponding sense amplifier band in the standby cycle is fixedly determined and not changed in progress of the operation (“said specific memory block invariantly being designated” recited in claim 1, as amended). The reason is as follows: in Ooishi, a refresh address is used for selecting memory blocks, respectively, to be normally connected to and isolated from the sense amplifier band, in which a memory block to be isolated from a corresponding sense amplifier band is changed in accordance with the block designating address included in the refresh address.

Accordingly, Ooishi does not disclose a semiconductor memory device including “a bit line isolation control circuit for setting at least the bit line isolation circuit provided for a specific memory block to be nonconductive in a standby mode of operation, said specific memory block invariantly being designated,” (emphasis added). It is therefore submitted that Ooishi does not disclose all the limitations recited in claim 1, and therefore, does not have identical disclosure of each element of the claimed invention in the meaning of 35 U.S.C. §102.

It is noted that a dependent claim is not anticipated if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the

dependent claim. Therefore, claims 2, 4 and 5 are patentable because they respectively include all the limitations of independent claim 1.

Applicants, therefore, respectfully solicit withdrawal of the rejection of claims 1, 2, 4 and 5, and favorable consideration thereof.

Conclusion.

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Recognition under 37 C.F.R. 10.9(b)

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WDC99 959757-1.067161.0038

ANNOTATED SHEET

FIG.10

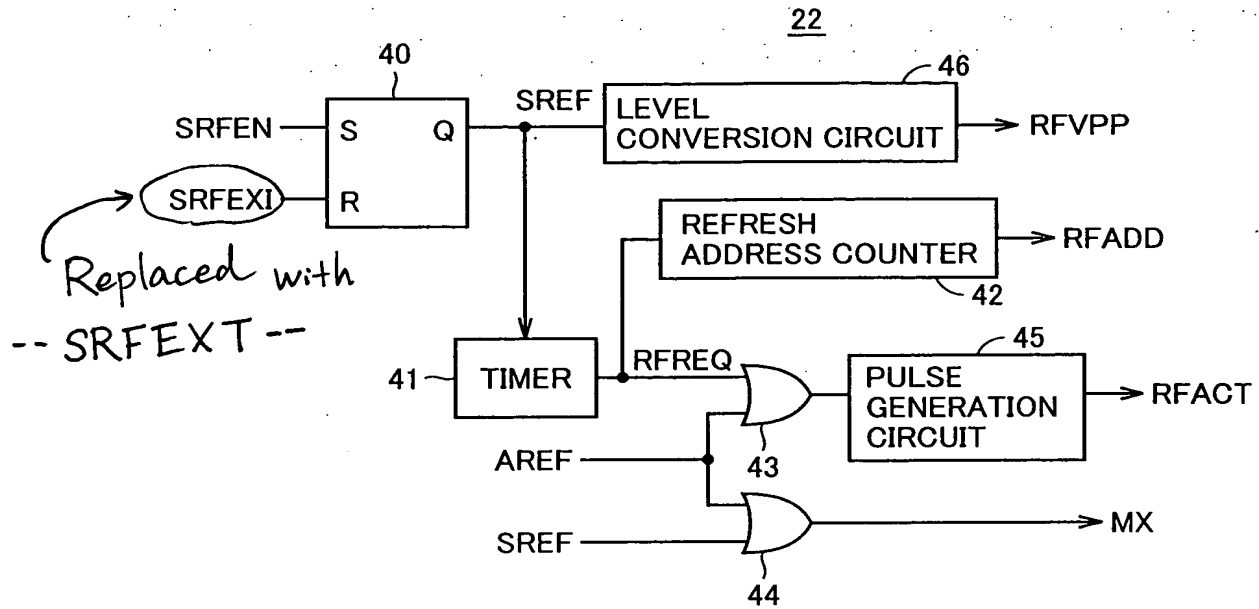


FIG.11

